REMARKS

Claims 1, 5-10, 26, 29, and 32-33 remain in the application. Claims 2-4, 11-25, 27, 28, and 30-31 have been cancelled.

By this amendment, applicants have amended claims 1 and 26 to more particularly set out the subject matter of the present invention. Applicants' FIGS. 1-4 and paragraphs [0013], [0023], and [0024] support the changes to claims 1 and 26. Additionally, claims 7, 29 and 32 have been amended to more appropriately depend from their respective independent claims.

Status of the Claims

In the *Disposition of the Claims* section of the present Office Action, it is stated that claims "1-5, 10, 26, 27, 29, 32, and 33" are pending the application. Applicants respectfully believe that the correct status of pending claims is: 1, 5-10, 26, 29, and 32-33. If applicants are mistaken in that regard, applicants respectfully request further clarification.

Response to the 35 U.S.C. §112 Rejection

Claims 7, 10, and 32-33 were rejected under §112, second paragraph because it was unclear what material applicants are referring to for the layer of material overlying the walls of the second trench.

Applicants respectfully submit that this layer of material can be separate from the polycrystalline semiconductor layer called out in claim 1 and the polysilicon cap layer called out in the claim 26.

Specifically, applicants respectively call the Examiner's attention to FIG. 4 and layer number **95**, which is shown in this embodiment as a separate layer from polycrystalline semiconductor layer **75**.

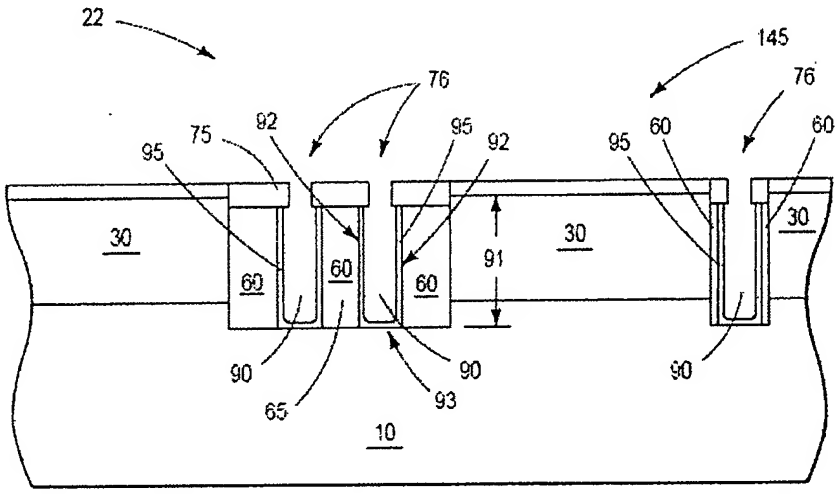


FIG. 4

Layer 95 is further described in paragraphs [0023] and [0024], where applicants specifically describe polysilicon and amorphous silicon as examples of materials for layer 95. Polysilicon and amorphous silicon are both types of polycrystalline silicon material.

Thus, in view of the above, applicants respectfully submit that claims 7, 10, and 32-33 meet the requirements of 35 U.S.C. §112, second paragraph, and respectfully request the withdrawal of this rejection.

Response to Prior Art Rejections

Claims 1, 5-8, 26, 29 and 32 were rejected under 35 U.S.C. §102(e) as being anticipated by Akatsu, et al., USP 6,333,274 ("Akatsu"). This rejection is respectively

traversed in view of the amendments made herein and the remarks presented hereinafter.

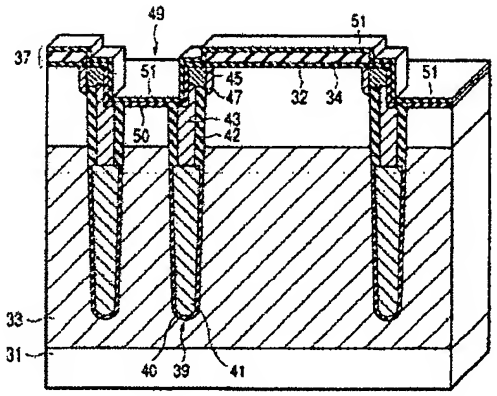
Claim 1 calls for an intermediary of a semiconductor device including a semiconductor substrate (see e.g., FIG. 1 elements 10 and 30), which has a surface formed with a first trench (see e.g., FIG. 1 element 20). A first dielectric material is formed in the first trench (see e.g., FIG. 2 element 60), and the first dielectric material substantially fills the first trench (see e.g., FIG. 2). A polycrystalline semiconductor layer is formed overlying the first dielectric material and has a first opening (see e.g., FIG. 3 elements 75). A second trench is etched into the first dielectric material through the first opening (see e.g., FIG. 4 element 76). The second trench has walls, a lower surface and a second opening (see e.g., FIG. 4). The first opening at least partially overlies the second opening (see e.g., FIG. 4), and the polycrystalline semiconductor layer and the second trench are configured to form a region of reduced substrate capacitance (see e.g., FIG. 6, element 22).

Applicants respectfully submit that the Akatsu reference fails to anticipate claim 1 for at least the following reasons:

1. Akatsu does not teach a first trench substantially filled with a first dielectric material. In the present Office Action, the Examiner points to Akatsu's element 49 as the first trench, and element 50 as the first dielectric material. However, as clearly shown in FIG. 2J and further described at Col. 4, lines 53-54, layer 51 is only 100

Angstroms thick, and certainly does not substantially fill trench 49.

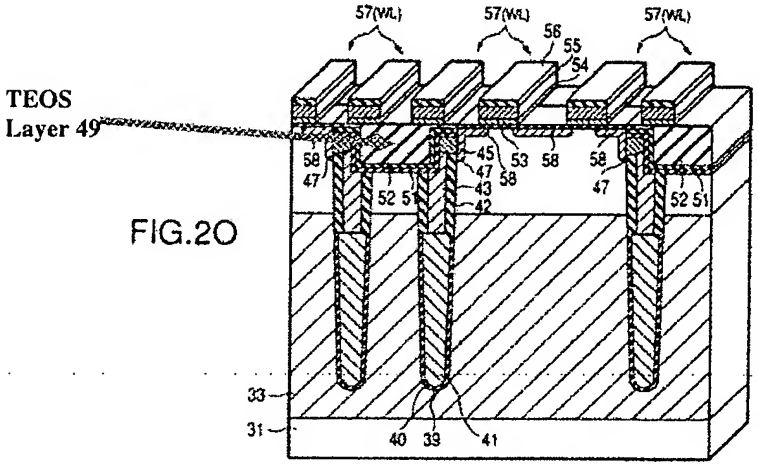
FIG.2J



Thus, Akatsu is missing at least this element of claim 1.

2. Claim 1 further calls for a polycrystalline layer formed overlying the first dielectric layer and formed with a first opening. A second trench is etched into the first dielectric layer through the first opening. Applicants respectfully submit that this latter element is missing as well from Akatsu. In particular, as shown in FIG. 2O:

FIG.2O



dielectric liner 50 is buried deeply below TEOS layer 49, and although there are openings between word lines 57 that include polysilicon layers 54, no second trench is etched into the first dielectric layer through such openings as required in claim 1. Thus, applicants respectfully believe that claim 1 allowable for this additional reason.

3. Further, Akatsu's polysilicon layer 54 is not configured to form a region of reduced substrate capacitance. It is simply configured as a part of a word line structure, and nothing more. Thus, applicants respectfully believe that claim 1 is allowable for this further reason.

Claims 5-8 and 10 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

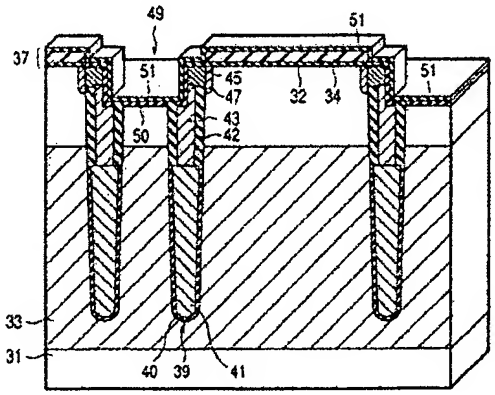
Claim 26 calls for an intermediary of a semiconductor device, including a semiconductor substrate (see e.g., FIG. 1 elements 10 and 30) having a surface formed with a first trench (see e.g., FIG. 1 element 20). A first dielectric material is deposited in the first trench (see e.g., FIG. 2 element 60), and the first dielectric material substantially fills the first trench (see e.g., FIG. 2). A polysilicon cap layer is formed overlying the first dielectric material and has a first opening (see e.g., FIG. 3 elements 75). A second trench is etched into the first dielectric material through the first opening (see e.g., FIG. 4), and the second trench has a second opening adjacent the first opening (see e.g., FIG. 4, element 76). The polysilicon cap layer and the second trench are

configured to form a region of reduced substrate capacitance (see e.g., FIG. 6, element 22).

Applicants respectfully submit that the Akatsu reference fails to anticipate claim 26 for at least the following reasons:

1. Akatsu does not teach a first trench substantially filled with a first dielectric material. In the present Office Action, the Examiner points to Akatsu's element 49 as the first trench, and element 50 as the first dielectric material. However, as clearly shown in FIG. 2J and further described at Col. 4, lines 53-54, layer 51 is only 100 Angstroms thick, and certainly does not substantially fill trench 49.

FIG.2J



Thus, Akatsu is missing at least this element of claim 26.

2. Claim 26 further calls for a polysilicon cap layer formed overlying the first dielectric layer and formed with a first opening. A second trench is etched into the first dielectric layer through the first opening. Applicants respectfully submit that this latter element is missing as well from Akatsu. In particular, as shown in FIG. 2O:

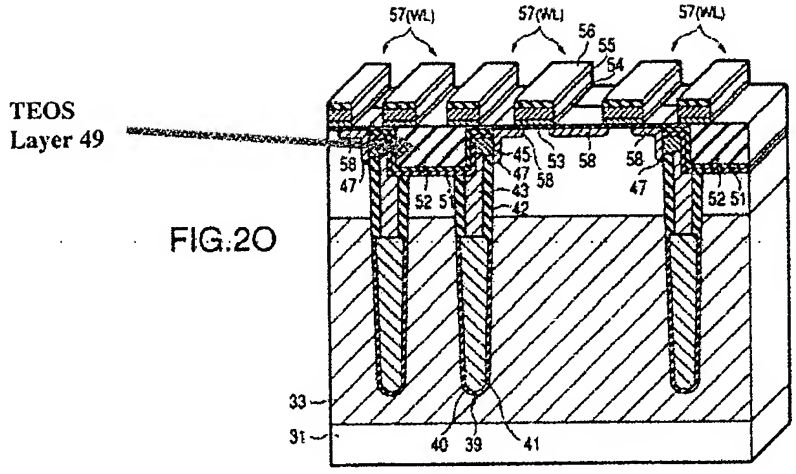


FIG.2O

dielectric liner 50 is buried deeply below TEOS layer 49, and although there are openings between word lines 57 that include polysilicon layers 54, no second trench is etched into the first dielectric layer through such openings as required in claim 26. Thus, applicants respectfully believe that claim 26 allowable for this additional reason.

3. Further, Akatsu's polysilicon layer 54 is not configured to form a region of reduced substrate capacitance. It is simply configured as a part of a word line structure, and nothing more. Thus, applicants respectfully believe that claim 26 is allowable for this further reason.

Claims 29 and 32-33 depend from claim 26 and are believed allowable for at least the same reasons as claim 26.

Claim 9 was rejected under 35 U.S.C. §103 as being unpatentable over Akatsu.

Claim 9 depends from claim 1. As stated above, Akatsu does not show or suggest a first trench substantially filled with a first dielectric material; a second trench etched into the first dielectric layer through the first opening in a polycrystalline semiconductor layer; nor a polycrystalline semiconductor layer configured to form a region of reduced substrate capacitance. Thus, in view of its dependence on claim 1, claim 9 is believed to be allowable over Akatsu for at least these reasons.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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